PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : G09F 9/37

A1

(11) International Publication Number: WO 92/12506

(43) International Publication Date: 23 July 1992 (23.07.92)

(21) International Application Number: PCT/GB92/00002

(22) International Filing Date: 2 January 1992 (02.01.92)

(30) Priority data:
9100188.3 4 January 1991 (04.01.91) GB

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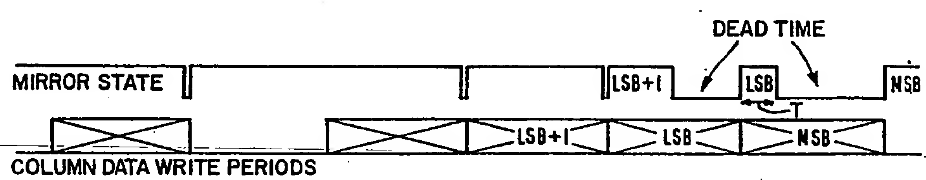
(81) Designated States: AT (European patent), BE (European patent), CA, CH (European patent), DE (European patent), DK (European patent), ES (European patent), FR (European patent), GB, GB (European patent), GR (European patent), IT (European patent), JP, KR, LU (European patent), MC (European patent), NL (European patent), SE (European patent), US.

Published
With international search report.

(54) Title: DISPLAY DEVICE



(57) Abstract

A display device comprising a plurality of deformable mirror devices arranged in a matrix array (20) to reflect light from a source (22) to a receiver (24) when in an on state, arranged to display grey level intensity values in response to digital input signals by switching the modulators on or off for periods corresponding to the significance of bits of a digital grey scale input word, in which there are provided dead time intervals in which the modulators are in a reset condition during which bit data can be written to the array (20).

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DISPLAY DEVICE

This invention relates to a display device (or a similar output device such as a matrix printer) of the type comprising an array of electrically switched light modulating devices, and to a method of operating such a device.

One type of electrically switched light modulator is the deformable mirror device described in "Deformable-Mirror Spatial Light Modulators", Hornbeck, published in the proceedings of SPIE Volume 1150 on 6-11 August 1989 in San Diego, California, USA. EP 0332953, 0385705, 0385706 and 0391529 also describe such devices. In this type of device an optical reflector is mounted on a torsion element over a surface mounted control terminal, so that applying a field between the reflector and the terminal causes the reflector to pivot against the action of the torsion mounting. In use, a display device comprises a plurality of such modulators arranged as an array with a light source arranged to illuminate the display so that, from a viewing position or optical pick-up, the light reflected from each modulator is related to the deflection of the modulator. It is possible to use such a device to effect a continuous

quantitative light modulation, by applying an analog signal level within a certain range to the electrode, in which case the deflection is a function of the analog level. The present invention is, however, concerned with devices which are operated to have discrete modulation states. In such devices, each modulator appears either bright or dark (e.g. ON or OFF) depending upon its discrete state.

In a digital device where it is desired to display grey scale images, one solution is to utilise the integrating response of the human eye by controlling the time for which the display device is switched on. In one particular scheme used in liquid crystal light modulators, described in GB 2014822 for example, this is arranged by accepting the signal to be displayed in a binary digital form, for example of 8 bits, and then operating the device in a on/off state over eight periods (or, in general, a number of periods which corresponds to the number of bits) the bit periods being of different lengths, the state of the device (ON or OFF) in each of the periods being responsive to the state of a corresponding one of the bits.

The length of the least significant bit (LSB) period is fixed and predetermined, and the length of the next most significant period is twice as long, and so forth, so that the length of the most significant bit period is 128 times that the of the least significant bit period. In general, for an N bit binary word, the length of the most significant bit period is 2^N-1 times the LSB period Provided that all the periods take place within a display frame of less than around 20 msecs duration, the human eye will integrate the periods and respond as if to a single period having a level of brightness corresponding to the binary signal value. The brightness is thus given by $\sum_{i=0}^{N} b_i \, 2^{i-1} t_{LSB}$, where t_{LSB} is the least significant bit period. In this display device, the modulators are operated in a bi-stable manner so that each modulator is stably latched in its display state throughout a bit period, enabling the signal for the next bit period to be is supplied to its control terminal in the meantime. At the end of each bit period, a resetting signal is supplied to all modulators to switch them into the state which corresponds to the next bit signal previously supplied to their control terminal.

It will thus be seen that, because the state of each modulator is latched during each bit period, the bit data to be displayed in the next period is in each case loaded in the bit period which precedes it. The bit periods are of unequal length and the shortest bit period is that for the least significant bit, which in the known proposal is scale 1/255 of the frame repetition period for an eight bit grey scale. Since the frame repetition period is generally less than 20 msecs, the length of the least significant bit period is typically less than 78 usecs and in this time data comprising one bit for each of the display modulators (typically on the order of 500 x 500 modulators arranged as a display) must be transmitted so that the data rate is on the order of MHz. This high data rate is undesirable, and if the data rate is limited by some physical constraint such as capacitance of address lines, it is easily seen that the data rate will therefore constrain the minimum length of the least significant bit and hence the number of bits available in each frame period to represent brightness (in other words, the grey scale resolution).

The present invention provides a display, or similar, device employing an array of elements of this type in which the display circuitry is such that, following at

least the least significant bit period, there is provided a further period of time in which the elements are inactive and during which data is written to the elements.

Viewed in another way, the invention consists in providing a display or similar device of this general type in which during a bit period, bit data relating to the next bit period is written to the control terminals of the elements, in which the state of the elements is reset at the end of the bit period but data continues to be written to control terminals thereafter.

In another aspect the invention consists in providing an array of light modulators capable of operating in either a bi-stable or a tri-stable condition and means for selecting one of said conditions at one point of a display cycle and the other during another point.

The invention can provide a substantial increase in the time available for writing data to the display, enabling either lower data rates or a higher resolution (number of bit periods) to be used. However, this is achieved without additional switching operations so that there is no loss in the useful device lifetime.

The invention provides also corresponding methods of operating such devices. Other aspects and embodiments are as described, with advantages which will be apparent from the following description.

The invention is particularly applicable in projection display systems as described in our International Applications published as WO91/15923 and WO91/15843, which are incorporated herein by reference in their entirety.

The invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1 shows schematically a light modulator used in one embodiment of the invention;

Figure 2 shows schematically an array of such light modulators comprising a display device;

Figures 3A and 3B illustrate the basis of bi-stable and tri-stable operation of the modulator of Figure 1;

Figure 4 shows the timing of signals in a device according to a known proposal;

Figure 5 shows the general form of a display device of a known proposal;

Figure 6 shows in greater detail the addressing circuitry of the device of Figure 5;

Figure 7 shows the timing of signals in a device of this general form;

Figure 8 shows the timing of signals in a device according to one embodiment of the invention;

Figure 9 shows the timing of signals in a device according to a further embodiment of the invention;

Figure 10 shows a timing circuit for use in that embodiment of the invention.

Referring to Figure 1 a light modulator of the type referred to in the aforementioned Hornbeck paper comprises a torsion beam 2 in the form of a plate, supported by a torsion rod 4 which in turn is supported

at its ends (not shown). A substrate 6 carries a pair of control terminals 8, 10 symmetrically disposed around the axis of the torsion beam 2 defined by the torsion bar 4. The control terminals 8, 10 are connected to addressing lines (not shown) and a voltage is supplied to one or other. Also provided on the substrate 6 are a pair of landing electrodes 12, 14 disposed under the edges of the torsion beam 2. On the outer surface of the torsion beam is a reflective coating. The landing electrodes 12, 14 are electrically connected to the torsion beam 2, which is conductive, and is connected to a bias voltage line.

Each modulator has individual control terminal lines connected to the control terminals 8, 10, and all the bias voltage lines connected to the beam 2 and landing terminals 12, 14 are connected in common to a bias voltage source.

In use, generally speaking, the application of a voltage to one control terminal 10 will set up an electric field between the control terminal 10 and the torsion beam 2; the voltage supplied to the control terminal 10 is generally such that the field is attractive. The beam 2 therefore tends to rotate through an angle α towards the

control terminal 10 depending upon the magnitude of the field. The torsion bar 4 tends to resist any such rotation. If the field is sufficiently strong the beam 2 will be drawn to make physical contact with the landing electrode 14; to avoid unwanted discharge the two are connected in common. The magnitude of the attractive field is controlled therefore by the bias voltage V_b applied to the beam 2 and by the voltage applied to the control electrode 10. It would be possible to simultaneously apply a voltage to the other control electrode 8, but in practice this is avoided; two voltages in the same sense would produce a net compressive or tensile stress rather than a turning moment in the beam 2, and this is undesirable because stresses can reduce the useful life of the modulator.

Referring to Figure 2, a display device 20 comprises an array of modulators according to Figure 1 arranged as a rectangular matrix of m rows by n columns, each modulator providing one picture element (pixel). A method of manufacturing a plurality of such modulators on a common substrate is disclosed in the Hornbeck paper referred to above and in, for example, US 4566935 or US 4710732. A light source 22 is provided to illuminate the

display 20, and a light receiver 24 (a pupil lens, or merely a viewing station for the human eye) is positioned so that for any modulator, light from the light source 22 will be reflected to the receiver 24 when the modulator is in a first state (the "ON" state) and will be reflected to an area other than the receiver are 24 when the modulator is in a second state (the "OFF" state). At any instant, therefore, during a display, certain modulators will be in the ON state and certain modulators will be in the OFF state so that the <u>instantaneous</u> picture received at the receiver 24 will comprise a black and white image.

As described in our International applications WO91/15843 and WO91/15923, the light source 22 may be a high powered lamp and the light receiver 24 may comprise a projection lens system to direct modulated light to a display screen for viewing; three arrays may be provided, one for modulating each primary colour for a colour display system.

Referring to Figures 3a and 3b, the manner in which each modulator is arranged to operate will now be described briefly (for a fuller description, the reader is referred to the aforementioned prior art). Figure 3a shows a

graph of potential energy, on the vertical scale, against the deflection angle α (normalised, with the angle at which the beam 2 rests upon the landing terminals 12, 14 taken as $\pm$ unity). When the bias voltage V_b applied to the beam exceeds a negative voltage level V_1, which depends upon device geometry, the potential energy is lowest when the beam rests upon one of the landing electrodes 12, 14, as shown in Figure 3a. The central position, with the beam 2 parallel to the substrate 6, is unstable as are all intermediate positions. Thus, with the bias voltage V_b in excess of V_1, the beam 2 remains stably latched resting upon one of the landing electrodes 12, 14 each of which defines one of the ON and OFF conditions of the modulator, and will remain latched until the bias voltage V_b is removed, regardless of the value of the voltages on the control terminals.

Referring to Figure 3b, by way of contrast, when the bias voltage V_b is 0 volts the potential energy is lowest with the beam 2 lying parallel to the substrate 6 and applying increasing voltage to one of the control terminals 8, 10 has the effect of producing a corresponding increasing deflection from the parallel state towards a respective

one of the landing electrodes 12, 14 so that when a sufficiently high voltage is applied to one of the control electrodes the beam 2 is brought into contact with the corresponding landing electrode. However, this state is unstable in the sense that any reduction of the voltage V_b on the control electrode will allow the beam 2 to once more move towards the stable parallel orientation.

Also illustrated in Figure 3B is the case where the bias voltage V_b applied to beam 2 exceeds a threshold V_2 but does not exceed the bi-stable threshold V_1. When the bias voltage V_b lies within this range, the potential energy of the system exhibits three minima; a central minimum with the beam 2 lying parallel to the substrate 6, and minima with the beam 2 lying in contact with each of the landing electrodes 12, 14. In this state, if the bias voltage is applied to the beam 2 when it is in any one of these three positions, the position will remain latched regardless of the value of voltage on the control terminals 8, 10. The modulator thus acts as a tri-stable

latched device when the bias voltage V_b is in this range.

Referring to Figure 4, the method of operation of a modulator in a digital grey-scale display device 20 will now be described. The state in which the beam 2 rests upon the landing terminal 14 will be described as the "ON" state, and that in which the beam 2 rests upon the landing electrode 12 will be described as the "OFF" state; these states are induced respectively, by a voltage (V_{ON}) supplied to the control electrode 10 and a voltage (V_{OFF}) of the same value supplied to the control terminal 8. When in the "ON" condition, the modulator reflects light to the receiver 24. Imagine, for simplicity, that a video signal to be displayed upon the display 20 comprises a plurality of pixel values each comprising four bits defining, in binary form, the intensity of light at each picture element of the display 20. For example, the light intensity may be 11/16 of the white value, represented in binary as 1011. The modulator state is switchable at intervals defining four bit periods B_3, B_2, B_1, B_0, during which period the modulator state is latched. The period B_0 is the shortest

and corresponds to a single notional clock period. If the least significant bit of the word is set, as is the case in this example, the modulator will be in the "ON" state during this bit period. The next-most significant bit period B_1 lasts twice as long and if the corresponding bit of the luminance word is set (as is here the case) the modulator is in the ON state during this period. B_2 and B_3 are respectively 4 and 8 times as long as B_0. As shown, the modulator is responsive first to the most significant bit. Since this is set, the modulator remains in the ON state for eight clock cycles. Since the next-most significant bit is not set, the modulator is switched to the OFF state for the next four clock cycles. Since the next bit is set the modulator remains in the ON state for two cycles and since the least significant bit is set, the modulator remains in the ON state for an additional one cycle. Thus, over 15 cycles the modulator is ON during 11; since the sum of all the bit periods is less than the response time of the eye, the appearance of the modulator from the reception area 24 is at a corresponding grey level of 11/16 the maximum possible luminance.

It will, of course, be appreciated that the order in which the various bits are "displayed" is entirely arbitrary for the purposes of the present invention, but in the following description the convention of displaying the most significant bit first and subsequent bits in order of significance will be adopted.

To switch the modulator, to the most significant bit value a positive voltage (of, typically, a few volts for compatability with TTL circuits) is supplied to the ON control terminal 10 and the voltage on the OFF control terminal 8 is set to 0 volts. The bias voltage V_b applied to the beam 2 is maintained at a negative value in excess of V_1 so that the modulator is bi-stable and the beam 2 remains locked in its present state regardless of the changes in the voltages on the control terminals. Just prior to the initiation of the most significant bit period, the bias voltage is brought to 0 volts (or, at any rate, to a level less than V_2).

If the state of the modulator has changed, neither the bias voltage nor the electrostatic field from the control terminal relating to the state in which it was previously held will influence the beam 2, which therefore swings up

through the parallel state and inclines somewhat towards the ON control terminal 10. Since occasionally moisture may provide a "stiction" adhesion force trapping the beam 2 on the landing electrode, it may be desired to provide an additional brief reset pulse as described more fully in the Hornbeck paper discussed above to the beam 2 to assist in separating it from the landing electrode. At a time sufficient to allow the beam 2 to settle the bias voltage V_b is then reapplied to the beam 2; since the beam 2 is now inclined towards the ON state terminal 10 when the bias voltage is reapplied, the stable state is reached when the beam 2 rests upon the ON state landing terminal 14. The modulator is now stably in the ON state and the voltage V_{ON} applied to the control terminal 10 may be removed at any convenient time period.

At some convenient point prior to the end of the most significant bit period B_3, the bit data concerning the next bit B_2 is written to the modulator. In this case, since the next bit is a 0, a positive voltage is supplied to the OFF state terminal 8 (and, if not done already, the ON control terminal 10 is set to 0 volts). This has no immediate effect because the bias voltage V_b is still

applied so the modulator remains latched in the ON condition. At, or just prior to, the end of the most significant bit period B_3, the bias voltage V_b is reduced as discussed before to allow the beam 2 to break contact with the ON state landing terminal 14, pass through an angle parallel to the substrate 6 and incline towards the OFF state terminal 8. Upon reapplication of the bias voltage V_b to the beam 2 shortly thereafter, the beam is therefore pulled down to the OFF state landing electrode 12 setting the modulator into the OFF condition.

As before, shortly prior to the end of the bit period B_2 the modulator receives the data enabling it to switch to the ON period for the subsequent bit period B_1; in other words, a positive voltage is supplied to the ON state control terminal 10 and the voltage is removed from the OFF state control terminal 8; and then, the bias voltage is reduced for a time period sufficient to enable the beam 2 to break contact with the OFF state landing electrode 12 and incline towards the ON state control electrode 10. Subsequent reapplication of the bias voltage therefore switches the modulator back into the ON state. At the end of this bit period B_1, the same

process occurs except that since the modulator is to remain in the ON state the voltages applied to the control terminals 8, 10 are not changed and upon re-application of the bias voltage V_b the beam 2 returns to the ON state landing terminal 14 whence it came.

It will be evident from the foregoing that in fact the voltages V_{ON} and V_{OFF} applied to the terminal 8, 10 need only be applied during the period for which the bias voltage V_b is pulsed off; while the bias voltage is applied, the voltages present on the control terminals are irrelevant. These voltages may therefore be applied as pulses of limited duration commencing before and finishing after the period during which the bias voltage is pulsed off.

Referring to Figure 5, the general operation of an array 20 of modulators will now be explained. In the array 20, the beam 2 and landing electrodes 12, 14 of each modulator are all connected commonly to a bias voltage supply terminal fed from a system clock 50. The two control terminals 8, 10 (e.g. are connected in a conventional matrix addressing network), by row and column lines so that each modulator may separately be

written to. The two control terminals 8, 10 may be logically inter-connected so that when one is on the other is off, and controlled from a single address line. The row and column lines are connected to an address generator circuit 52 of any convenient type. An incoming digital video signal generally comprises a serial bit stream which represents, say, eight bits of one picture element followed by eight bits of the next adjacent element in a row, and so on in a row scanned format. The clock rate of the signal is extracted to synchronise with the display clock circuit 50. The bit stream is then supplied to a bit reordering circuit 54, which generally comprises at least a frame store and suitable addressing logic, and the bit stream is reordered so that all most significant bits for each pixel are supplied first to the address circuit 52, followed by all next most significant bits, and so on. The bits are then written to the modulators making up the display 20 in some convenient scan pattern during the bit period B_{i-1} immediately preceding the bit period B_i to which they relate. At the expiry of the bit period B_{i-1}, all the bits B_i for the next bit period will have been written to to their corresponding modulators and the clock 50 brings the bias voltage line to ground to switch the

modulatorsover . No particular frame blanking period is necessary or provided. Thus, the most significant bits of the next frame must be written to the display 20 during the least significant bit of the preceding frame.

By providing a shift register or other first in first out (FIFO) device connected to each of the rows (or, alternatively, each of the columns) of the array 20, all modulators of a given row can be written to in parallel (as discussed below). However, even so, the time constraint imposed by this requirement to write bits to all modulators within the least significant bit period is severe; for example, employing an eight bit grey scale at a frame repetition period of 20 msecs the least significant bit length is approximate 78 usecs and during this time, even supplying bits to all modulators of a row in parallel, for an average resolution display having 576 rows the data rate required is (576/78) MHz = 7.4MHz. Achieving either higher resolution by employing more pixels as in proposed high definition television systems, or higher grey scale resolution by employing more bits per pixel, makes data rates unattractively high since the capacitance of addressing lines and other circuit components becomes significant.

Referring to Figure 6, in one embodiment the addressing circuit 52 comprises a plurality of FIFO registers 56a, 56b, 56c etc, each connected to a data line 57a, 57b, 57c which is connectable to the control terminals 8, 10 of each of the modulators of a single column. Row enable line 58a, 58b, 58c for each row of the array 20 are connected so that when a signal is placed on a row enable line the respective modulators of that row are connected to their respective column data lines 57a, 57b, 57c; this may conveniently be achieved, as shown, by connecting each row enable line 58a, 58b, 58c to the gate of a FET transistor interconnecting a modulator with its respective column line 57a. The row enable lines are connected to the outputs of a demulti- plexor 59 and sequentially selected by clocking the demultiplexor from the system clock 50. The clock 50 also clocks all the shift registers together. Thus, a row of bit values are written to each of the modulators of a given row and then the next row of bits are brought forward within the FIFOs 56a, 56c and written to the next row, until bits for all rows of the frame have been written to the display 20. The FIFOs 56a-56c etc then contain the next-most significant bits for the first row, ready to be written to the display 20 in the next bit period. Bits received

from the bit reordering circuit 54 are distributed to the FIFOs 56a-56c etc in sequence via a demultiplexor 60.

In a device according to an embodiment of the invention, the data rate constraint is alleviated as follows.

Referring once again to Figure 3b it will be recalled that when the bias voltage V_b is reduced below V_1, there is a potential energy minimum associated with the parallel position of the beam 2. The voltages supplied to the control terminals 8, 10 are insufficient to bring the beam 2 into one of the ON or OFF states in the absence of a substantial bias voltage. It is therefore possible to reset the beam into the central parallel position, in which the control terminal voltages may be altered with only a minor effect on the orientation of the beam insufficient to put it into the ON state. It is therefore possible to put all the beams of all the modulators into the parallel position by reducing the bias voltage, and thus switch off one bit period without commencing the next.

Referring to Figure 8, by contrast with Figures 4 and 7, the working of the invention will be demonstrated. After the least significant bit period, there is provided a further period of the same length in which no modulator is switched on. By contrast with the apparatus of the preceding Figures 4 and 7, the length of a single frame is now 256 times the length of the least significant bit period instead of 255 times the least significant bit period; this results in a 0.4% reduction in overall brightness, but has an advantage in that the lengths of all the bit periods are even fractions of the frame length so that all bit periods can be derived by dividing down the clock period by successive multiples of 2. During the "dead time" period following the least significant bit, the beam 2 of each modulator lies in the parallel state and the light source 22 and receiver 24 are so arranged that the parallel state does not reflect light into the receiver 24 and thus the modulator appears to be in the "OFF" state. During this period, the voltages applied to the control terminals 8, 10 do not cause the beam 2 to enter the ON state and so this period of dead time can be used to write the data to be used for the most significant bit period of the next frame. In other words, the effective time available for writing data in the worst case is almost doubled (2/256 instead

of 1/255). This effective halving of the data rate for a given resolution can be used either to increase the number of pixels by two, or the grey scale resolution by one bit, or to halve the data rate.

In the light of the foregoing, however, it will readily be appreciated that the principle of the invention can be extended to further reduce the required bit rate. Referring to Figure 9, the data rate may be halved yet again by providing an additional four dead time periods; two periods after the next-least significant bit but before the least significant bit and two more (making a total of three) following the least significant bit. There are now four least significant bit periods T available for writing bit data during least significant bit period and least but one most significant bit period; additionally, the period B_2 is already four least significant bit periods long and all other bit periods are longer than this. Thus, in the worst case, the time available for data transmission is 4/260 as opposed 1/255 in the method of Figures 4 and 7. The price to pay is a slight decrease in overall brightness since the maximum whiteness compared to the previous proposal is 255/260 instead of 255/255. However, the grey scale itself if

undistorted by the process since all the bit periods are still exactly related in length by multiples of 2. In general, for a clock rate reduction of 2^n it can be shown that the required display dead time is:

Dead time = $T.\overset{N}{\underset{0}{}}\Sigma n.2^{\wedge}(n-1)$ - - - - - (1)

This may be summarised in the following table:

N	-	Dead time	Loss 8 bit	Loss 10 bit
0	1	0	0%	0%
1	2	T	0.39%	0.098%
2	4	5T	1.96%	0.49%
3	8	17T	6.7%	1.66%
4	16	49T	19.2%	4.79%

In practice the errors will be slightly less than those calculated in the above table when the effects of the compression of the display time caused are taken into account. It can thus be deduced from the table that a 10 bit brightness resolution can be achieved at a burst data clock rate of 1/4 that of eight bit binary system which uses the arrangement of Figures 4 and 7, with only a 5% loss in peak brightness. In practice, the minimum least

significant bit period time, and hence the maximum binary display resolution, will be limited by the physical response time of the modulator device. Any drop in peak brightness can, of course, be compensated by increasing the power of the light source 22 commensurately.

It is thus seen that the invention has the effect of de-coupling the data rate from the length of the bit periods (specifically that of the least significant bit) by switching all modulators out of the ON state, writing to the modulators, and then allowing the modulators to take up the states corresponding to the data written to them. If necessary, all the bit periods could be separated one from the other by extended dead time periods during which writing takes place.

Referring to Figure 10, one particular implementation of the clock circuit 50 will now be described. A master data clock signal is derived from any convenient source (e.g. a crystal oscillator) and synchronised appropriately with the incoming data stream.

The time required to write data bits to all modulators is M master clock cycles (in the embodiment of Figure 6, this is equal to the number of rows if the master clock

runs at the bit transfer rate). The bit periods are set from a duration counter 100 which counts a number of clock cycles equivalent to each bit period length; the bit period lengths are held in successive locations in a ROM table 102 connected to the duration counter 100. At the end of a bit period, when the duration 100 counter counts down to zero, a modulator reset signal is generated which, as discussed above, removes the bias voltage and supplies a reset pulse to the beam 2 so as to cause the beam 2 to be switched to the parallel state (which appears to be "OFF" to the receiver 24). However, as discussed above, the next bit period is not necessarily instantly initiated; following some bit periods there will be a "dead time" interval.

During the down counting of the duration counter 100, at each step the count (remaining) is compared with M, the number of clock cycles required to write data to the display 20. When the count becomes equal to or less than M, a data counter 104 is enabled which counts M successive clock periods. Also enabled is a gate 106 which thereafter passes the clock signals to the address circuitry 52 to enable the data bits to be written to the display 20. When the data counter 104 has counted out M cycles, the transmission of data to the display 20 will

be complete. If the bit period was longer than M clock cycles (as it will generally be for the more significant bits), the duration counter 100 will also stop counting at this point but if the bit period was the least significant bit period, the duration counter will already have stopped since this period is shorter than M cycles. The data counter 104 then outputs a control signal which applies the bias voltage V_b to the beams 2 of the modulators of the display 20. The control signal also increments an interval counter 108 to indicate that the next bit period is to commence. The output of the interval counter 108 is coupled to the address lines of the ROM lookup table 102, which correspondingly puts the duration of the next bit period on its data output lines to be supplied to the duration counter 100, which starts running.

The circuit of Fig. 10 may be provided by discrete digital circuit components, or by a specially designed ASIC (application specific integrated circuit). However, a high speed microcomputer, or microprocessor or DSP device with associated ROM and RAM memory, may equally be employed to provide the circuit.

Means for generating voltage pulses of suitable values are well known in the art.

Where the present invention is employed in a system according to our above referenced PCT applications, the same timing circuit 50 may provide the timing for several different modulator devices, one for each primary colour of a colour projected display.

Whilst the invention has been described in relation to a display device, it will be understood also to be applicable to, for example, printer devices where light or other radiation is directed onto a surface to record an image.

CLAIMS:

1. An output device comprising a plurality of optical modulators physically moveable between two physical states corresponding to modulation states, and means for supplying data signals to the modulators to select said states, further comprising means for resetting the said modulators by switching them to a physical position intermediate said two physical states, characterised in that the means for supplying data are arranged to do so whilst the modulators are in said intermediate state.

2. A method of operating an output device comprising at least one light modulator switchable between first and second modulation states comprising the steps of: holding the modulator in one of said states for a predetermined time; at the expiry of said time, switching the modulator to a third state functionally equivalent to one of said first and second states; sending to the modulator a signal defining which of said first and second states is next to be output whilst holding said modulator in said third state; and switching said modulator to said next state.

3. An image output device comprising a plurality of light modulators having two stably latched modulation states in which data for a future state may be written to each modulator, in which each modulator has also a third stably latched state into which it is switched prior to being switched into the future state, and in which data for the future state may be written to it.

4. An output device comprising an array of light modulators capable of operating an either a bi-stable or a tri-stable condition in dependence upon a control signal, and means for supplying a control signal to select one of said conditions at one point of the display cycle and the other at another point of the display cycle.

5. An output device comprising a plurality of modulators each modulator having an ON state and an OFF state and control circuitry arranged to represent a multi-bit binary input value by setting the modulator to one of the states over a corresponding plurality of periods; each period having a length which corresponds to the bit to which the period relates; the state of the device in each bit period

being determined by the value of the corresponding bits; the control circuitry being arranged to write data relating to each bit to the modulators during display of the preceding bit; in which there are provided means for setting the modulators to an intermediate state at the end of one bit period and holding the modulators in said intermediate state whilst writing data thereto prior to setting the modulators to the next state.

6. A device according to any preceding claim, in which the modulators comprise reflectors movable between first and second reflection angles corresponding to said modulation states.

7. An output device comprising a plurality of deformable mirror devices each having two angular deflection states and means for holding each device in a central deflection state whilst writing data defining the next angular deflection state to the device.

8. A timing control circuit for use in setting the modulators of a device according to any preceding claim.

9. An output system comprising a timing control circuit according to claim 8 arranged to control a plurality of modulator arrays.

10. A display device according to any preceding claim.

FIG.1.

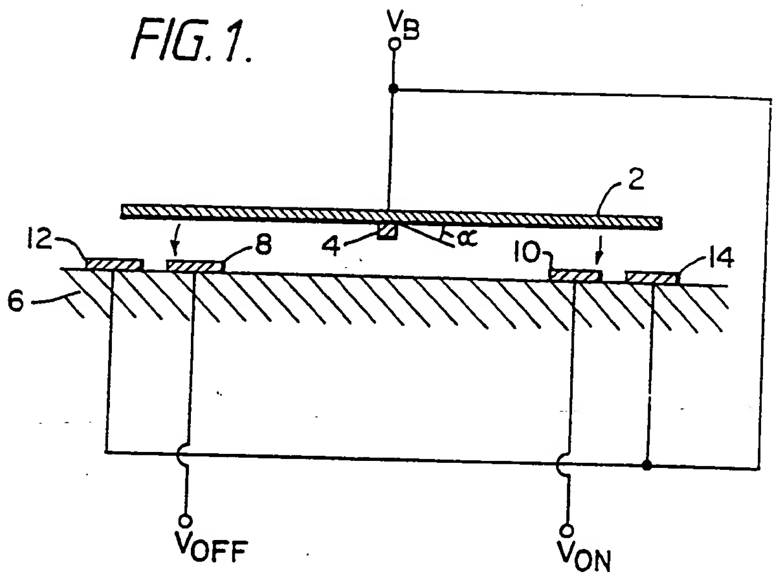


FIG.2.

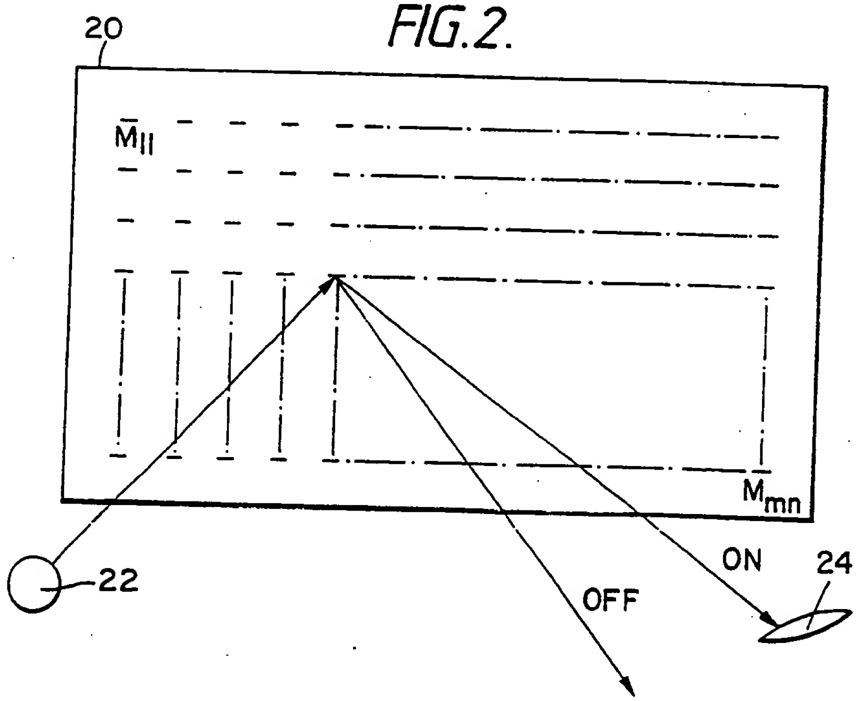


FIG.3A.

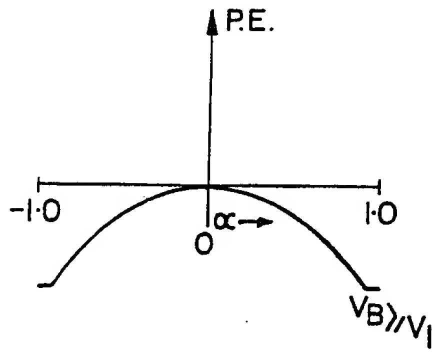


FIG.3B.

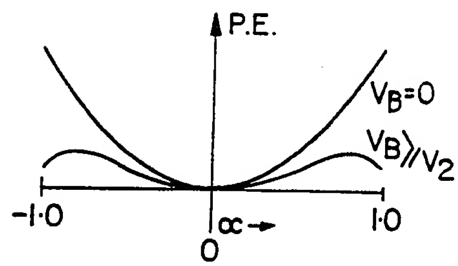


FIG.4.

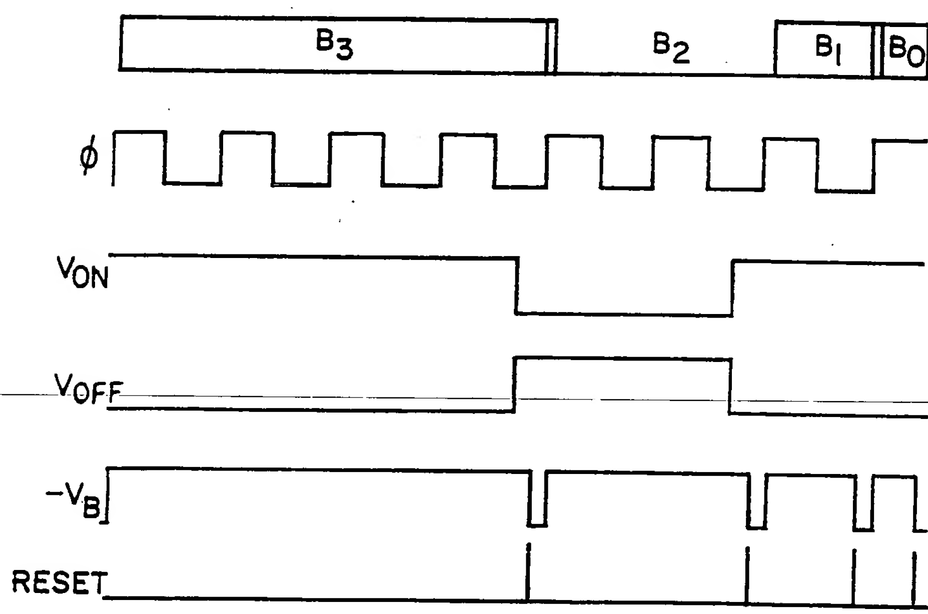


FIG. 5.

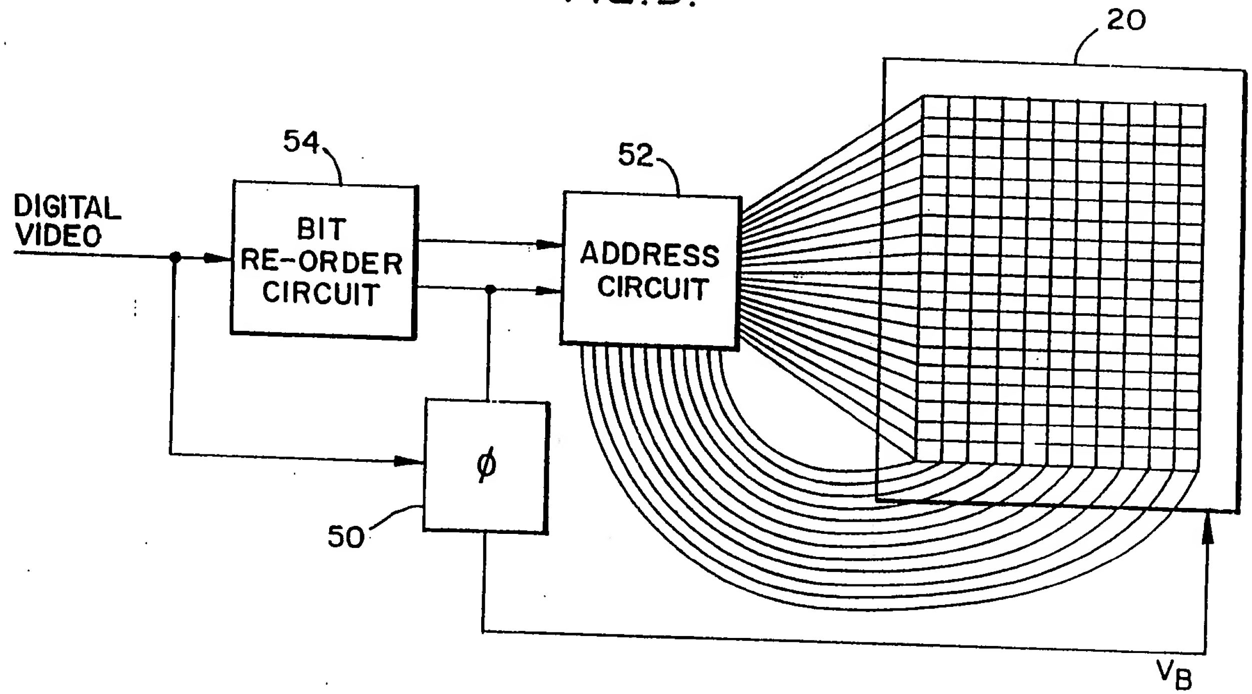

DIGITAL VIDEO
54
BIT RE-ORDER CIRCUIT
52
ADDRESS CIRCUIT
20
ϕ
50
V_B

FIG.6.

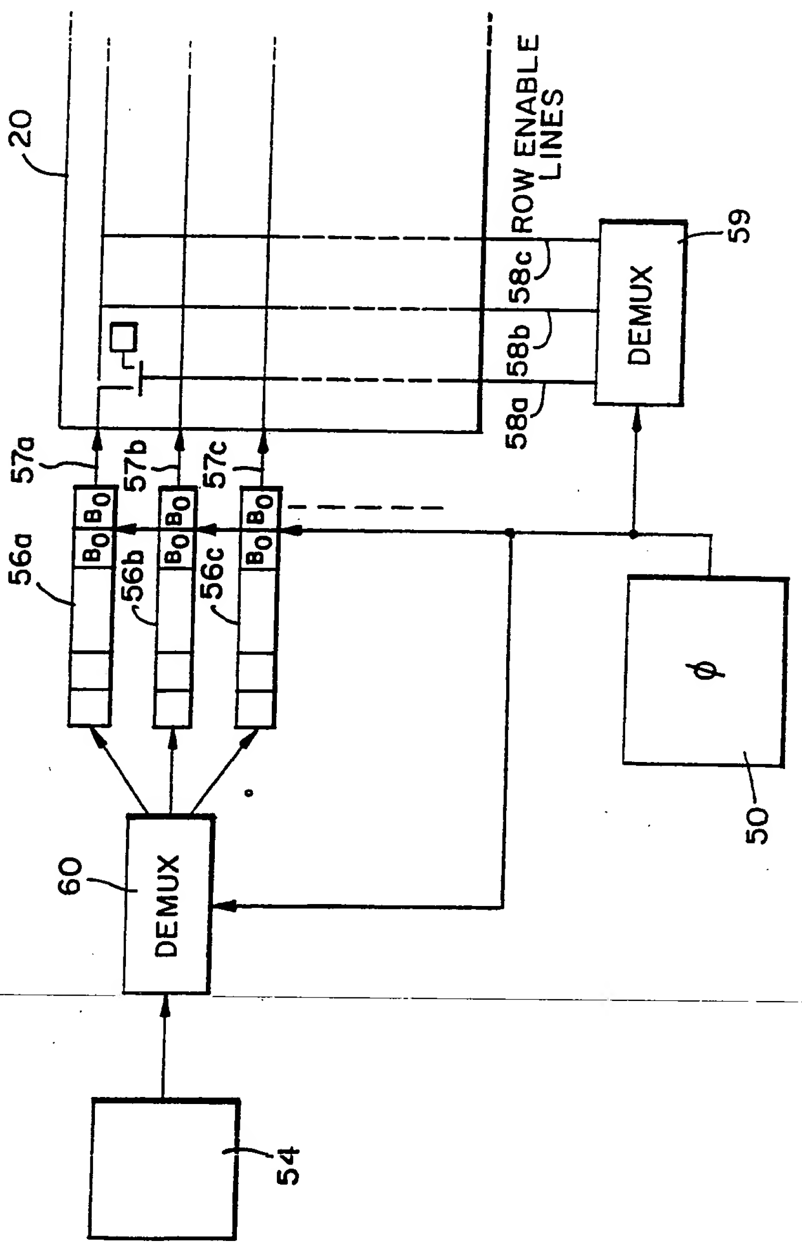

20
ROW ENABLE LINES
58a
58b
58c
59
DEMUX
57a
57b
57c
56a
56b
56c
B_0
B_0
ϕ
50
60
DEMUX
54

FIG.7.

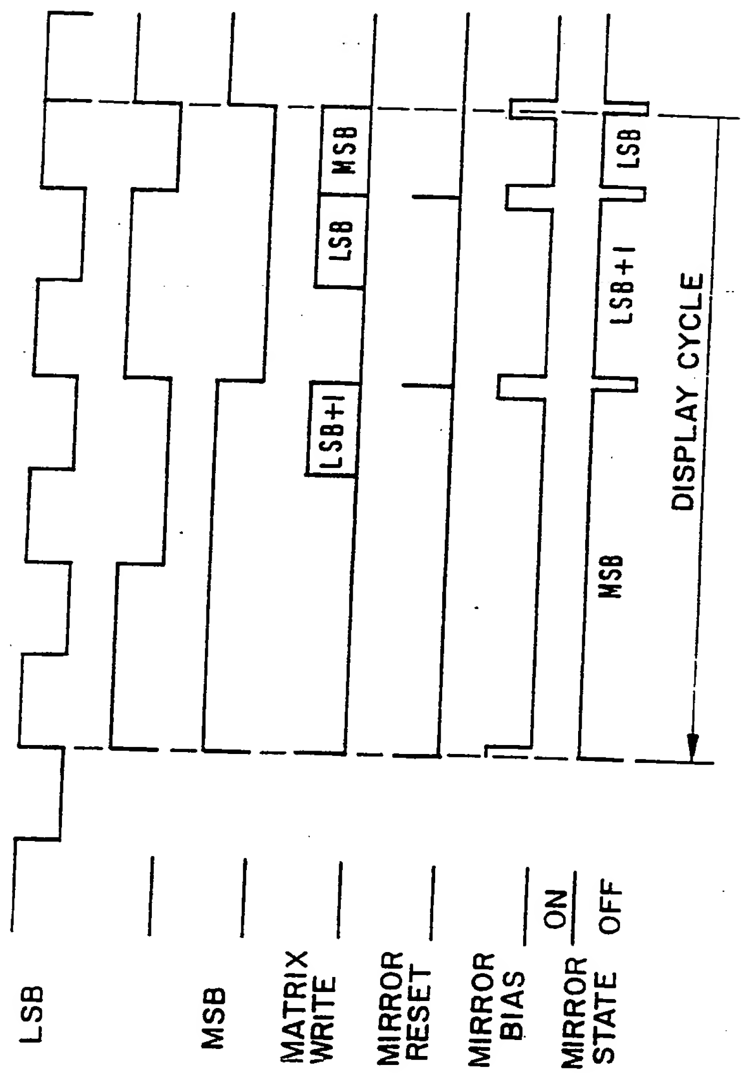

LSB
MSB
MATRIX WRITE
MIRROR RESET
MIRROR BIAS
MIRROR STATE
ON
OFF
LSB+1
LSB
MSB
MSB
LSB+1
LSB
DISPLAY CYCLE

FIG.8.

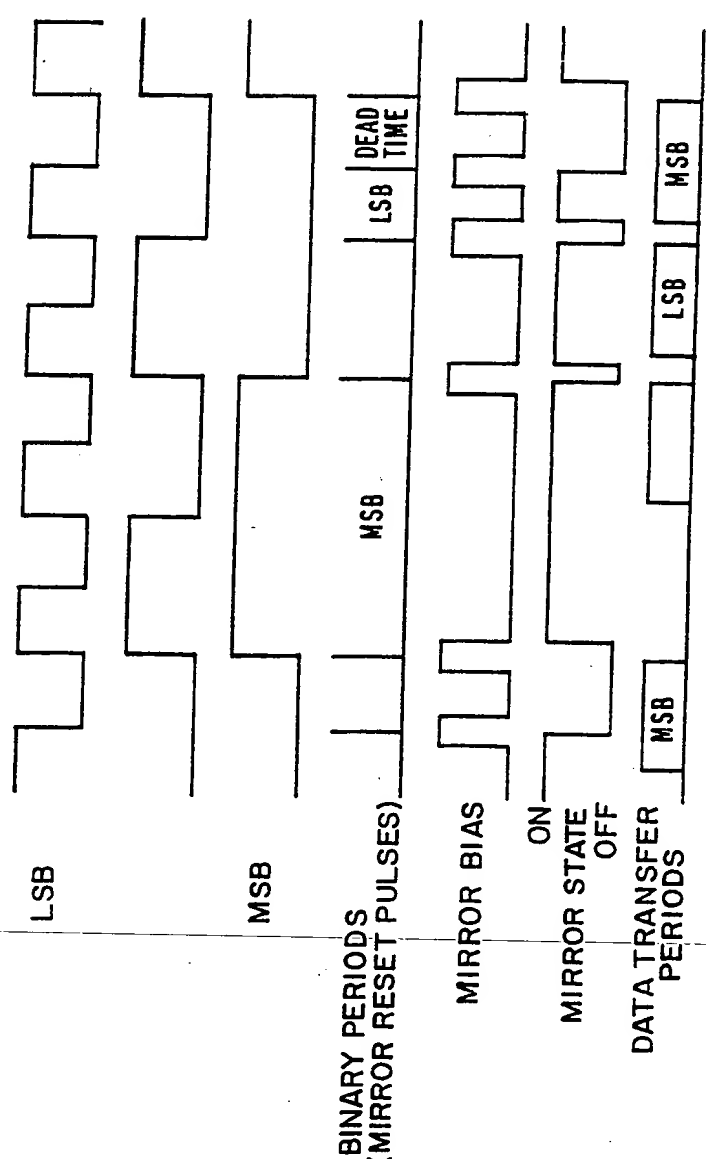

LSB
MSB
BINARY PERIODS
(MIRROR RESET PULSES)
MSB
LSB
DEAD TIME
MIRROR BIAS
ON
MIRROR STATE
OFF
DATA TRANSFER
PERIODS
MSB
LSB
MSB

FIG. 9.

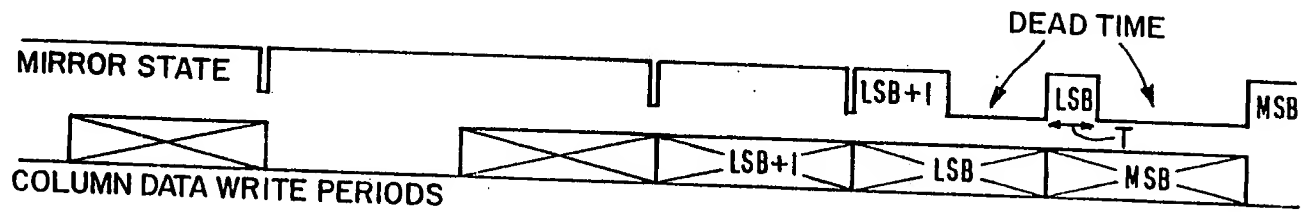
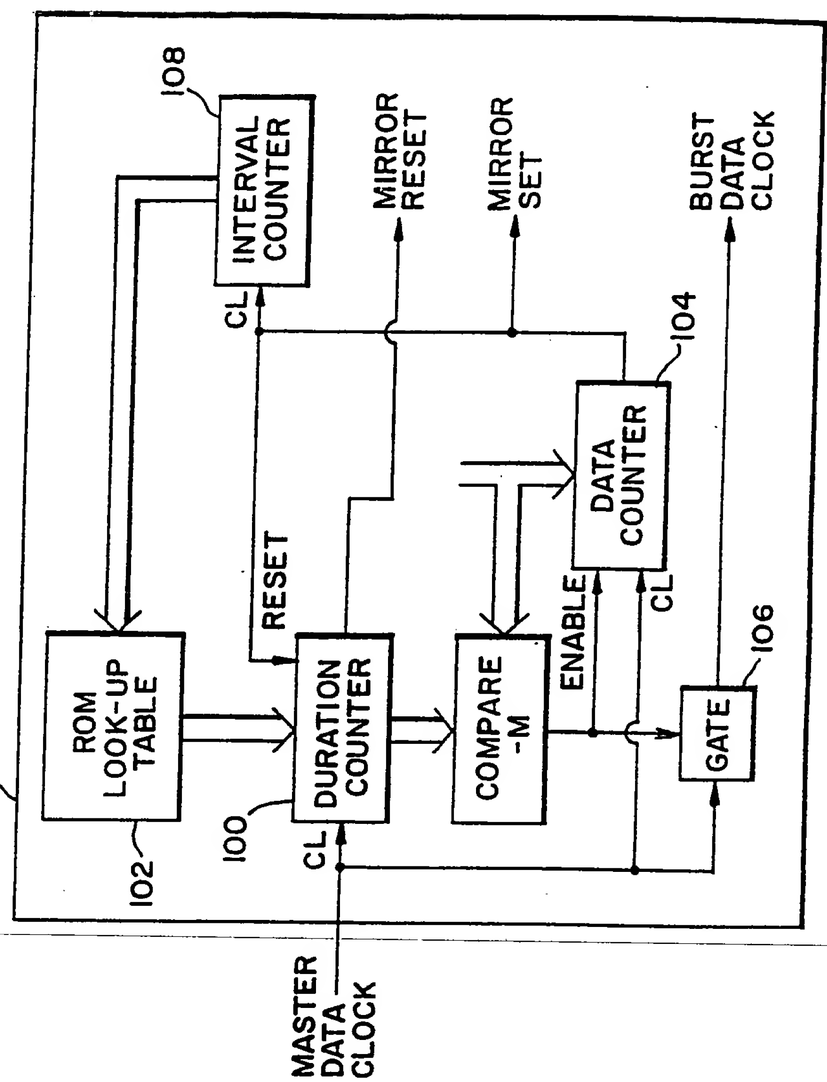

DEAD TIME
MIRROR STATE
LSB+1
LSB
MSB
T
COLUMN DATA WRITE PERIODS
LSB+1
LSB
MSB

FIG. 10.



50
ROM LOOK-UP TABLE
102
108
INTERVAL COUNTER
CL
RESET
DURATION COUNTER
100
CL
MIRROR RESET
MIRROR SET
COMPARE -M
ENABLE
DATA COUNTER
104
CL
GATE
106
BURST DATA CLOCK
MASTER DATA CLOCK

INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 92/0000

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC^5: G 09 F 9/37

II. FIELDS SEARCHED

Minimum Documentation Searched

Classification System	Classification Symbols
IPC^5	G 02 B 26/00, G 09 F 9/00, G 09 G 3/00, H 04 N 1/21

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched

III. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
P,A	US, A, 5 049 901 (GELBART) 17 September 1991 (17.09.91), see abstract. --	1
P,A	EP, A2, 0 433 985 (TEXAS INSTR.) 26 June 1991 (26.06.91), see abstract. --	1
A	GB, A, 2 014 822 (SONY) 30 August 1979 (30.08.79), see abstract (cited in the application). ----	1

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- "O" document referring to an oral disclosure, use, exhibition or other means
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- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- "&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
31 March 1992	15. 04. 92
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	Maria Peis Maria Peis

zum internationalen Recherchenbericht über die internationale Patentanmeldung Nr.

to the International Search Report to the International Patent Application No.

au rapport de recherche international relatif à la demande de brevet international n°

PCT/GB92/00002 SAE 54979

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This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The Office is in no way liable for these particulars which are given merely for the purpose of information.

La présente annexe indique les membres de la famille de brevets relatifs aux documents de brevets cités dans le rapport de recherche international visée ci-dessus. Les reseignements fournis sont donnés à titre indicatif et n'engagent pas la responsibilité de l'Office.

Im Recherchenbericht angeführtes Patentdokument Patent document cited in search report Document de brevet cité dans le rapport de recherche	Datum der Veröffentlichung Publication date Date de publication	Mitglied(er) der Patentfamilie Patent family member(s) Membre(s) de la famille de brevets	Datum der Veröffentlichung Publication date Date de publication
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